OAI Webinar Chapter 3:

E2E OAI 5G accelerated by the Xilinx T1 Telco card

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LDPC offload demo description

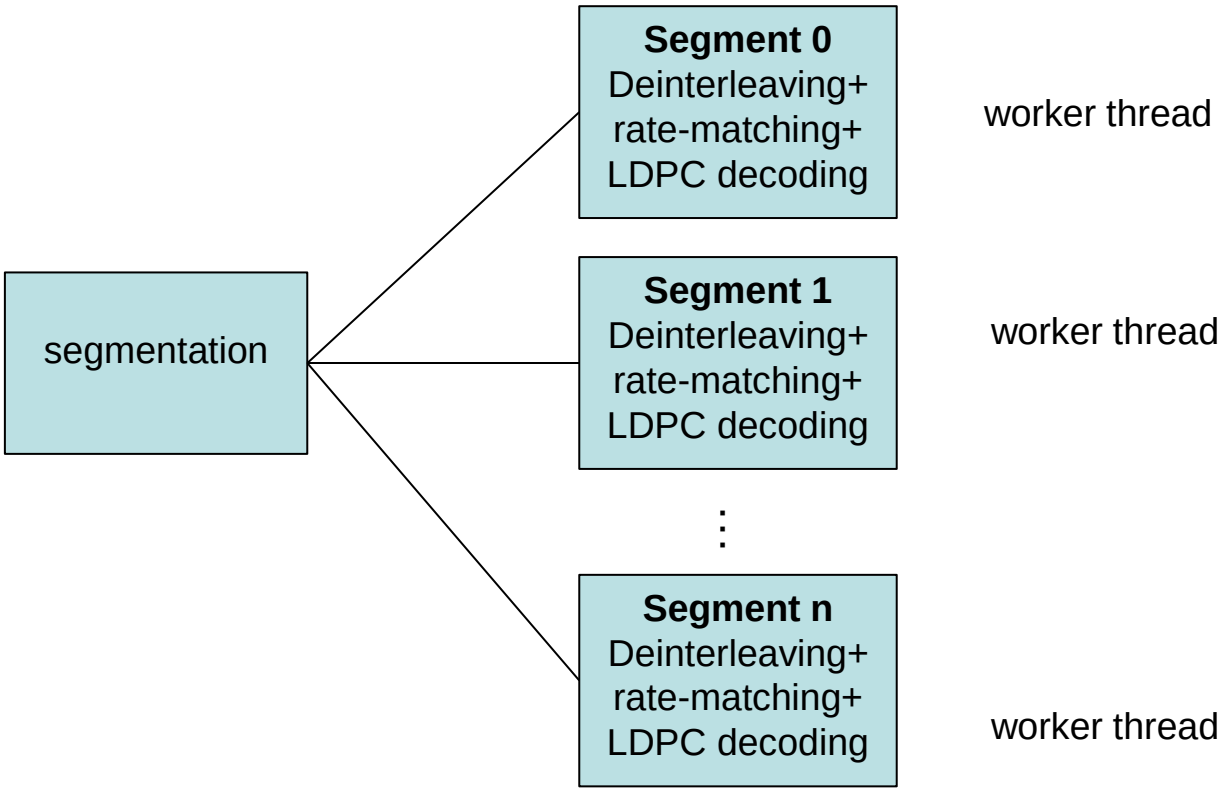
- The LDPC decoding is high computational consumption component. It is ideal candidate for offload to a FPGA. This demo shows the LDPC decoding can be offloaded to FPGA to reduce the CPU load. The 5G SA end-to-end transmission with the LDPC offload for channel decoding will be demonstrated.

- OAI today uses a thread-pool to decode the segments. The segmentation splits a transport block into multiple code-block segments. The segment process uses 3 decoding components: deinterleaving, rate-matching and ldpc decoding. Each segment decoding process runs on a different CPU core.

- The deinterleaving, rate-matching and LDPC decoding will be offloaded to Xilinx T1 card.

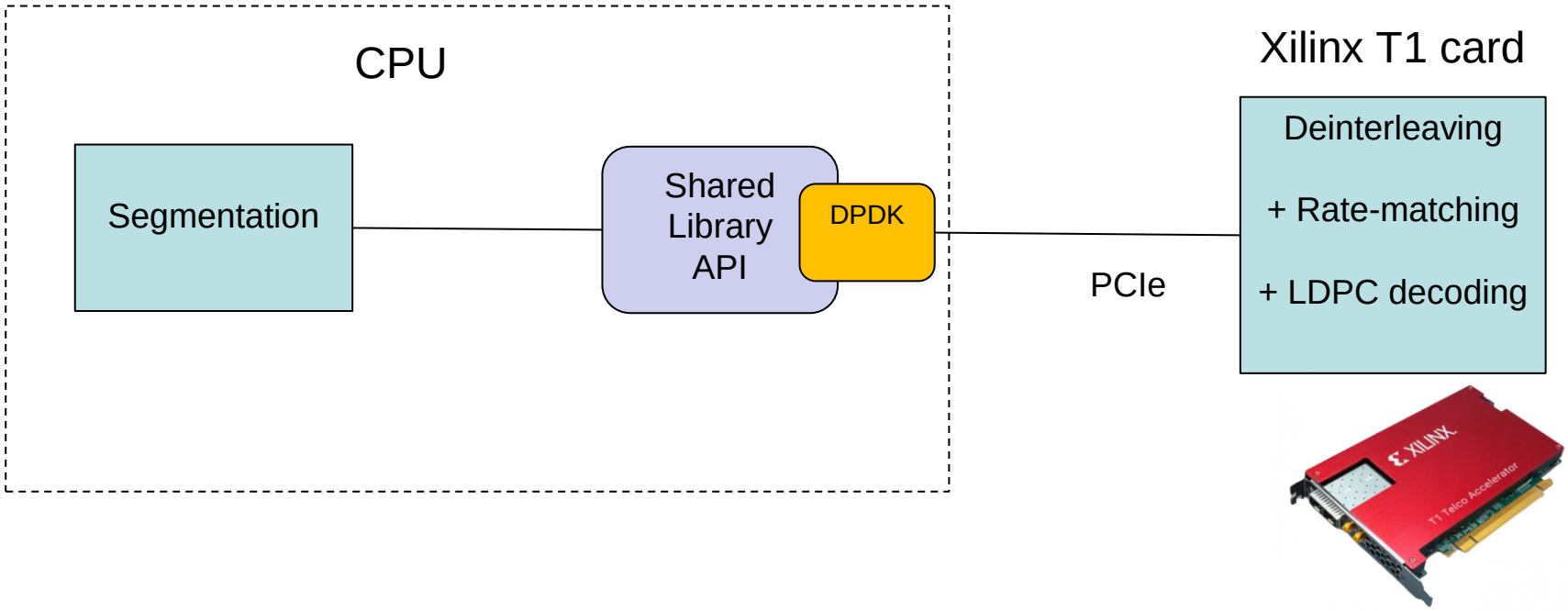
Current OAI ULSCH decoding chain

- `nr_ulsch_decoding.c:nr_ulsch_decoding()`
  - Segmentation : splits a transport block into multiple code-block segments
  - Each segment decoding process is managed by the routine `nr_ulsch_decoding.c:nr_process_ULSegment()`



LDPC Offload on Xilinx T1 card

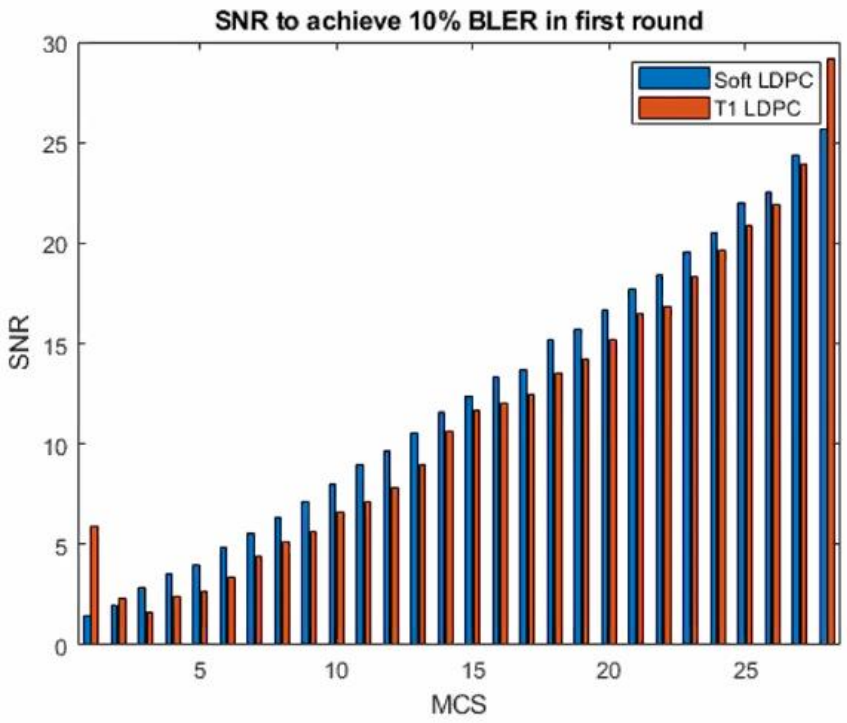
- A shared library is created to implement the interface for DPDK.
- The shared-library translates the OAI descriptors for ULSCH decoding into the required parameters for LDPC decoding used by the DPDK API.
- The mode 1 (CB mode) is used for T1 LDPC decoder.
- Branch name: ldpc_offload_t1_mr -> MR ongoing

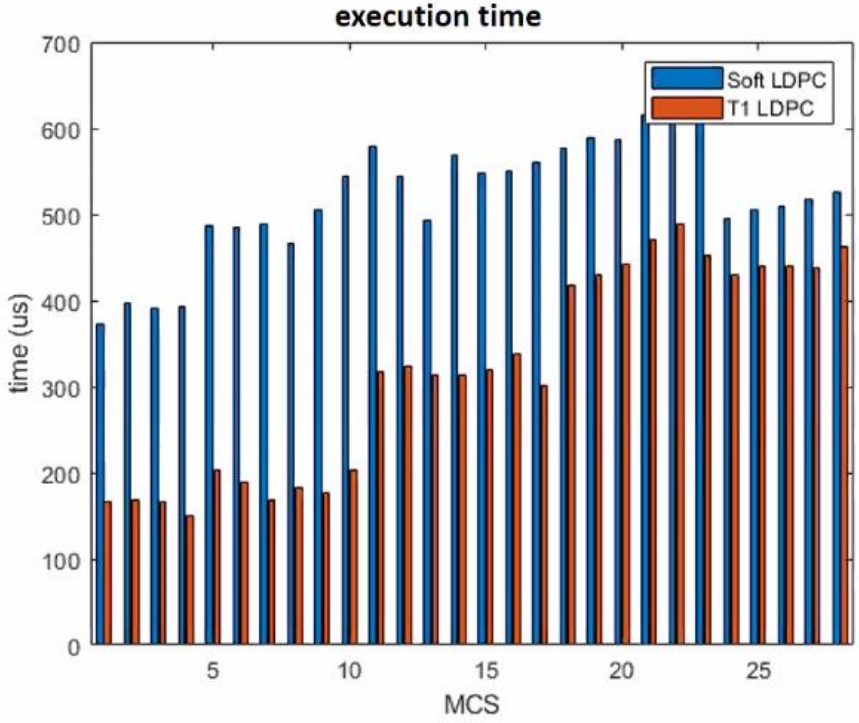


Demo configuration

- **5G SA end-to-end with commercial UE**
  - SCS 30kHz, 12 OFDM symbols, 2 DMRS, SISO
  - 60MHz BW
  - TDD configuration: 6 DL /1 SS /3 UL
  - COTS UE Quectel 500Q-GL

Uplink channel simulation results





NR-PUSCH, SCS 30kHz, 106PRB, 12OFDM symbols, 1 DRMS, SISO, TDL-C channel

Florian Kaltenberger, Hongzhi Wang, Saktivel Velumani, "Performance evaluation of offloading LDPC decoding to an FPGA in 5G baseband processing," Workshop on Smart Antennas (WSA2021), Sophia-Antipolis, France, 10-12.11.2021.

5G NR SA demo setup