

SCF FAPI Reference Implementation in OAI

- Opportunities for the Broader Community -

Andrei Radulescu / SCF FAPI chair

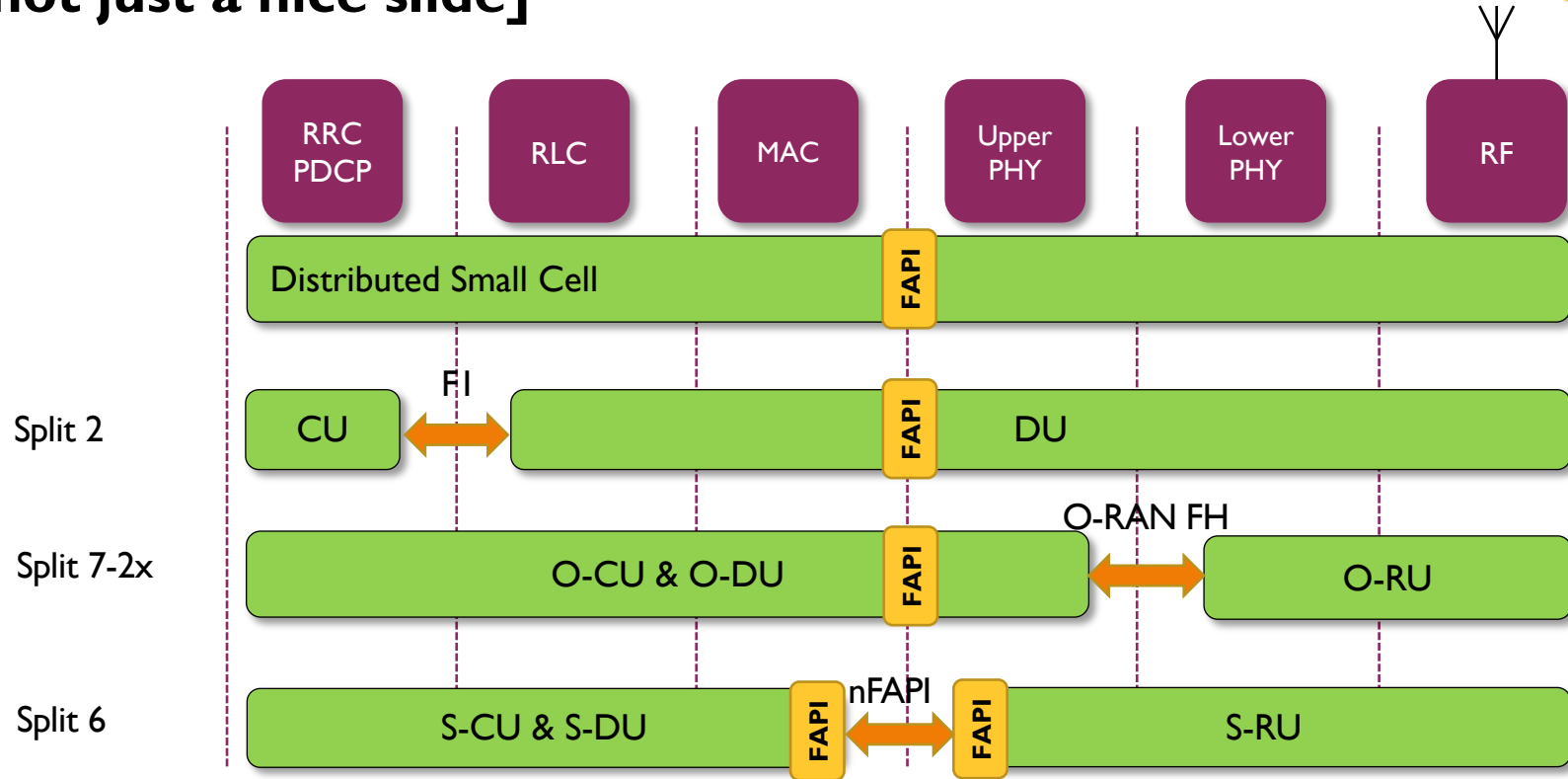
Nov 15, 2023



MOBILIZING
ENTERPRISES &
COMMUNITIES

FAP: Enabling Multiple Architectures

[not just a nice slide]





5G FAPI Ecosystem:

- diverse, mature, 3GPP, O-RAN compliant -

- **5G FAPIv2:** Focus on small cells



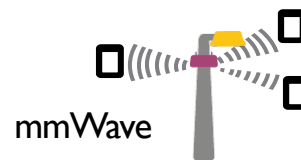
Semester releases

- **5G FAPIv7:** Mature specification ecosystem
 - Macro, Small, MIMO cells, FR 1/2.
 - Broad, Stable: Rel-15 and core Rel-16 support.
 - Diverse ecosystems of vendors and operators.
 - Standalone/S-RU, D-RAN, V-RAN.
 - Interworking with O-RAN FH.

Outdoor



Indoor



mmWave

sub-6GHz





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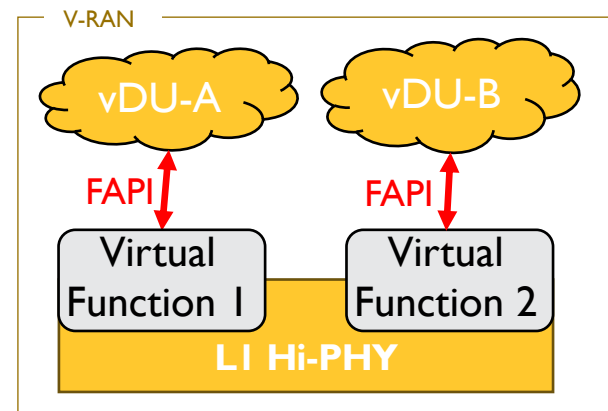
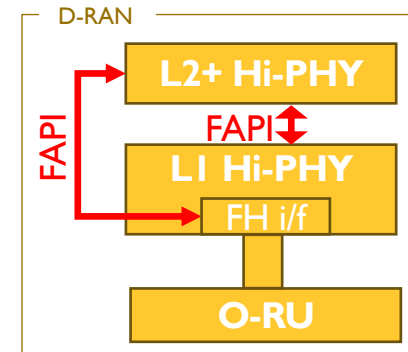
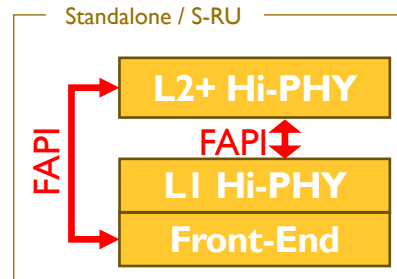
- **5G FAPIv2:** Focus on small cells



Semester releases

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- Macro, Small, MIMO cells, FR 1/2.
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- Healthy ecosystems of vendors and operators.
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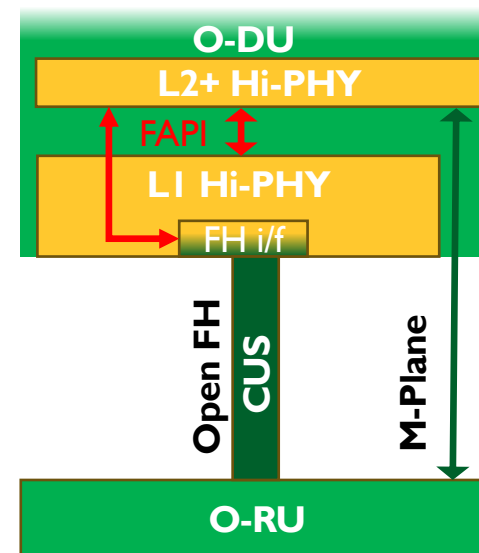
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SCF222 PHY FAPI/OAM Roadmap



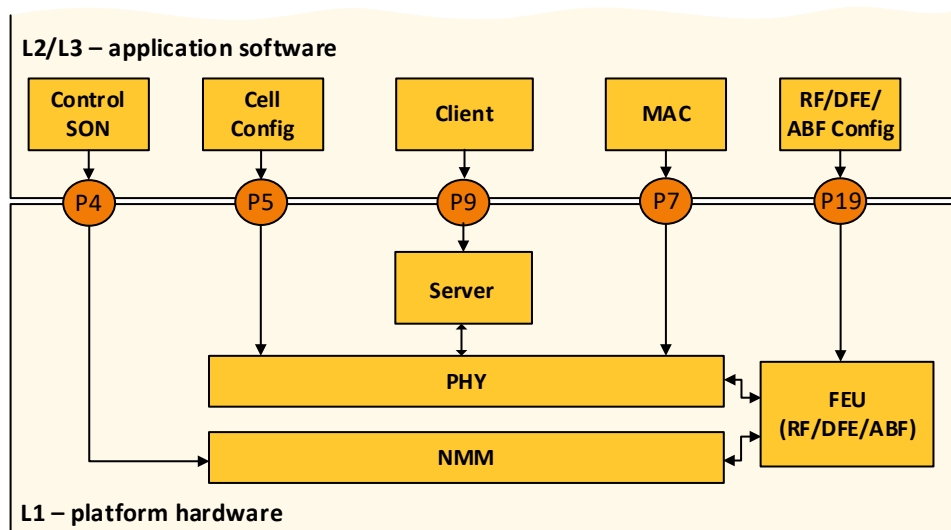
Q1/2020: v1,v2	Q2/2021: v3	Q4/2021: v4	Q2/2022: v5	Q4/2022: v6	Q2/2023: v7
<p>Rel-15 Support</p> <ul style="list-style-type: none"> PHY = Carrier P5: Config P7: Slot Operations <ul style="list-style-type: none"> DL Ctrl, Data & RS UL Ctrl, Data, RS, UCI Core support <ul style="list-style-type: none"> BWP, Coresets, flexible num-lgy, minislots, etc, 3GPP-based pwr profile Digital BF & precoding 	<ul style="list-style-type: none"> DL Rate Match, DSS Multi-SSB & RACH UCI Control CSG Retx [alternative] etc 	<ul style="list-style-type: none"> CBG re-tx • PRACH Offset Missing Capabilities TBS-TLV length • SR Len RSRP reports • TA etc 	<ul style="list-style-type: none"> SRS/MIMO PRACH power Mixed Numerology Pi/2-BPSK capability Failed-CRC TBS handling 	<ul style="list-style-type: none"> mMIMO Optimizations SR Payload General Corrections [mMIMO Beam Reporting & L2-based precoders] 	<ul style="list-style-type: none"> General Corrections EPRE definitions 3GPP/SCF Bitmap alignments CRBO, PRG definitions, etc
	<p>Rel-16</p> <ul style="list-style-type: none"> eMIMO (mTRP, MU-CSI) DSS 	<ul style="list-style-type: none"> eMIMO (low-PAPR RS) 2-Step RACH 	<ul style="list-style-type: none"> 2-Step Maintenance Positioning 	<ul style="list-style-type: none"> Maintenance (eMIMO, CSI) 	<ul style="list-style-type: none"> Maintenance (eMIMO, CSI, continued)
	<p>Features & Optimization</p> <ul style="list-style-type: none"> PUCCH-related pre-compute PDU counts; bit alignment SSS-based Pwr Profile Integration w/ P19, nFAPI-style headers 	<ul style="list-style-type: none"> mMIMO (SRS-based) CP/UP split Universal RM; signaling associations P7-based by-ref RM P7 Parameter Padding Transp. UCI for PUCCH SRS hop patterns 	<ul style="list-style-type: none"> 7.2x FH State Awareness Extended Errors Shared Memory for UL 64-bit pointers Config.reply TLV clarification 	<ul style="list-style-type: none"> RM Indexing O-RAN Alignment (P9) Multi-vDU Support PHY Profile (#antennas) Straight Wire Precoding 	<ul style="list-style-type: none"> O-RAN Alignment (P9 Notifications) Optimized signaling of 2-part CSI State machine restrictions
<p>General</p> <ul style="list-style-type: none"> Timing: SFN/slot sync State Machines P5 Configuration Procedures P7 Stateless operati 	<ul style="list-style-type: none"> Timing: Delay Management, SFN/slot Corrections Supervisory PHY 	<ul style="list-style-type: none"> Common Context nFAPI Headers Adaptation 	<ul style="list-style-type: none"> Timing: Delay Mgmt w/o Timestamps Explicit array sizes 	<ul style="list-style-type: none"> O-RAN Alignment: P9 Terminology, int16_t Delay Mgmt clarification 	<ul style="list-style-type: none"> Strict backward compatibility



FAPI Interfaces: not just about PHY Control

- P5/P7: PHY Control
 - In FAPIv2 OAI codebase.
- P4: NMM
- P19: Front-End control
- P9: OAM for O-RAN Fronthaul

RAN Internal Architecture



SON (Self Organizing Networks), MAC (Medium Access Control), NMM (Network Monitor Mode), FEU (Front End Unit), including DFE (Digital Front End) and ABF (Analog Beam Forming)

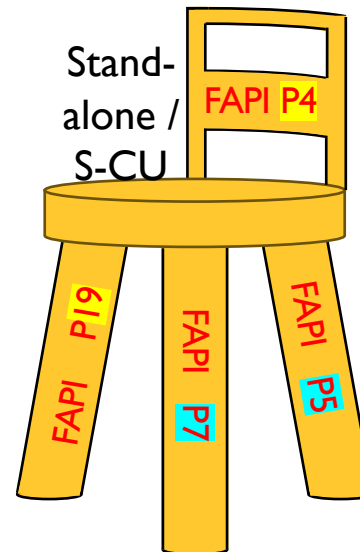
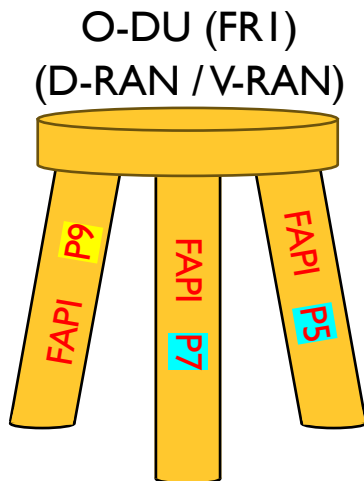


P5/P7: Immediate Open Sourcing Target

- SCF & OAI: agreed on maintaining an interface (in form of C header files), consistent with the SCF FAPI releases
 - Initial focus in P5/P7
 - General principles:
 - SCF owns and maintains FAPI Specifications
 - OAI will implement a Stage 3 FAPI API in the form of C headers
 - SCF and OAI will coordinate to ensure consistency and alignment under cooperation agreement
 - OAI will produce a Stage 3 reference implementation
 - Testing can build on OAI unit test cases and code (details TBD for future work)



FAPI-based LI architectures



- Legend:

- SCF & OAI Interfaces (P5, P7)
- SCF-only interfaces (P4, P9, P19)



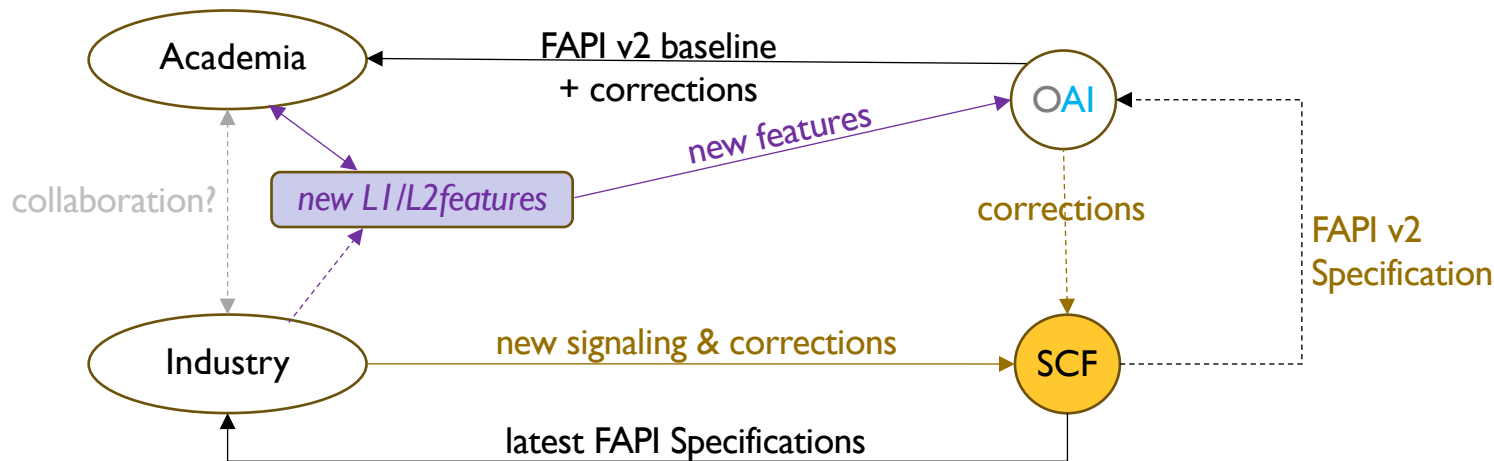
P9: Next Open-Sourcing Target?

- **P9: key enabler of O-RAN compatible architectures, with FAPI-based O-DU**
 - OAM between LI implementations and O-RAN architectures
- **Ripe for open sourcing:**
 - SCF-specified operations are defined using Google Protobuf
 - Data model uses O-RAN Open-FH M-Plane YANG modules, w/ SCFYANG extensions
 - Extensions help align port definitions and LI notifications



Community Opportunities

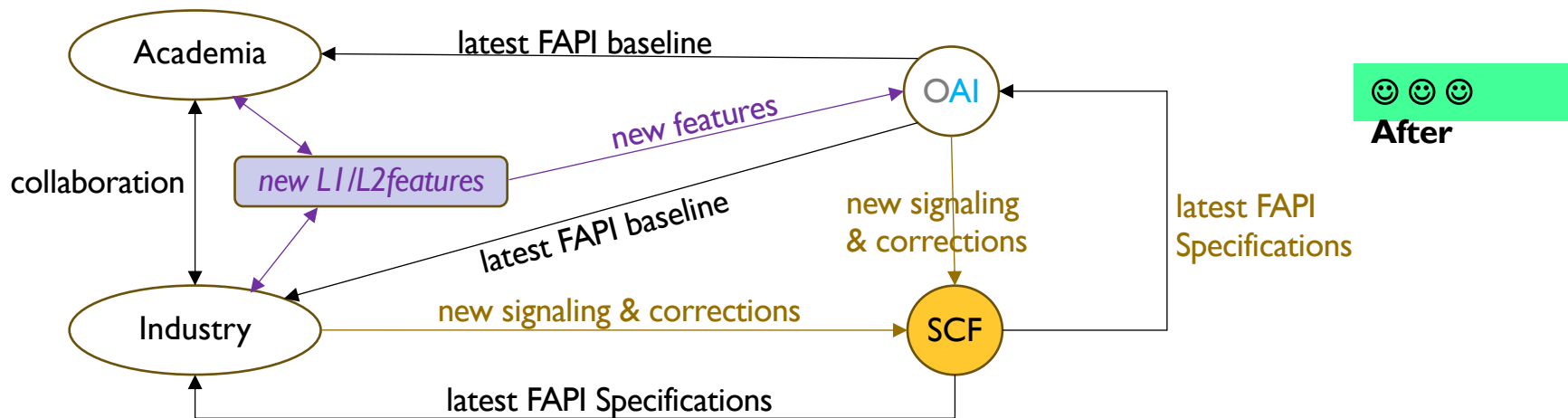
- OAI interfaces, with well-specified FAPI documentation => can focus on feature adoption, proposal and improvements.
 - FAPI header open sourcing reduces interface friction between SCF layers and across SCF/O-RAN interaction
- Virtuous cycle to use/add/improve features and contribute to specifications





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Community Opportunities

- Ecosystem build-up:
 - Rapid spec adoption => OAI codebase to remain fresh
 - FAPI backward compatibility => Safe to upgrade to latest specification
 - Building, tracking, testing, logging & tracing: => quality interfaces => focus on features.
- Open areas of collaboration: scheduling (MU-MIMO, multi-utility / URLLC), RIC assistance, Edge computing, NES, NTN, Testing, etc.



Thank you

Q&A



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